



FIG. 1A  
(PRIOR ART)

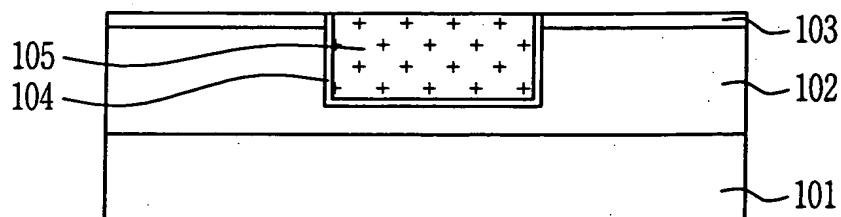


FIG. 1B  
(PRIOR ART)

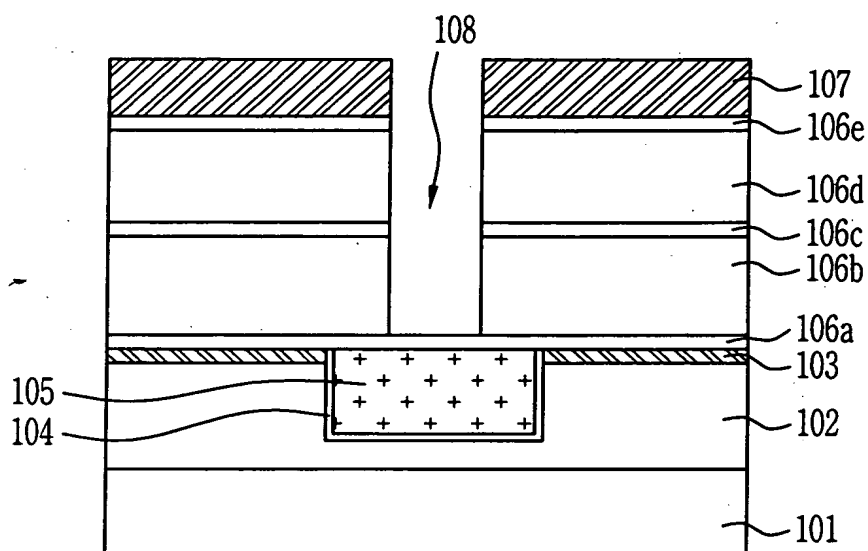
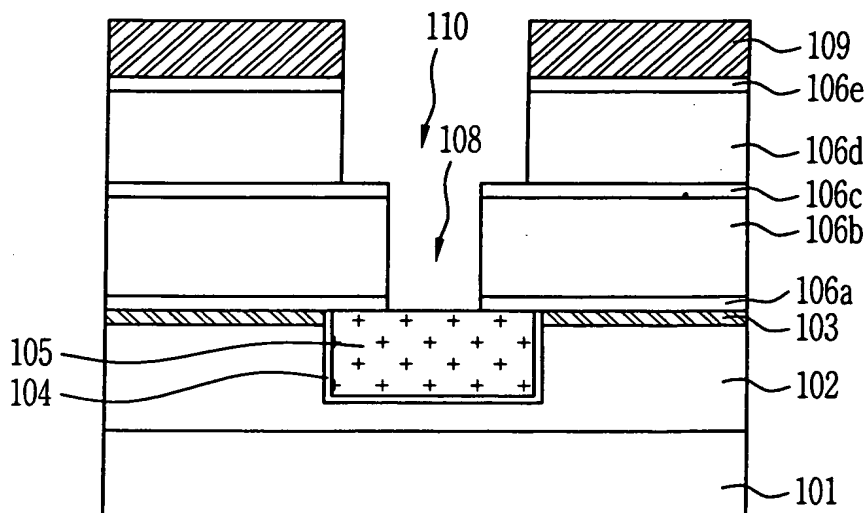


FIG. 1C  
(PRIOR ART)



(Replacement Sheet)

FIG. 1D  
(PRIOR ART)

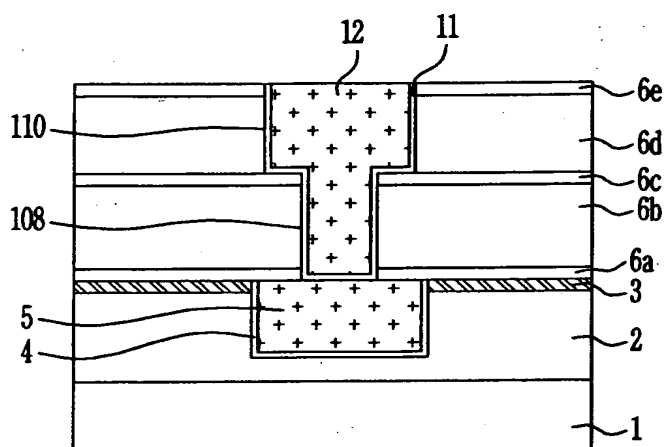


FIG. 2

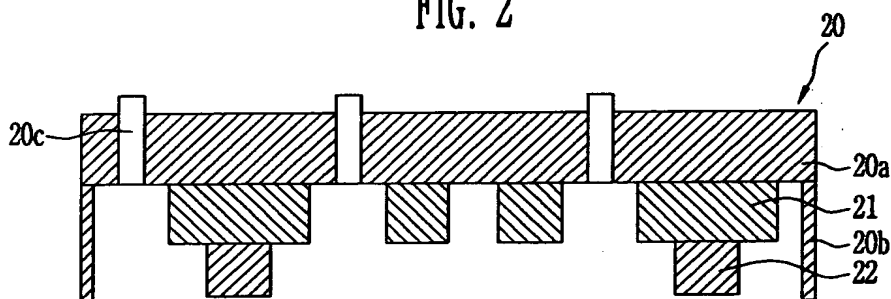
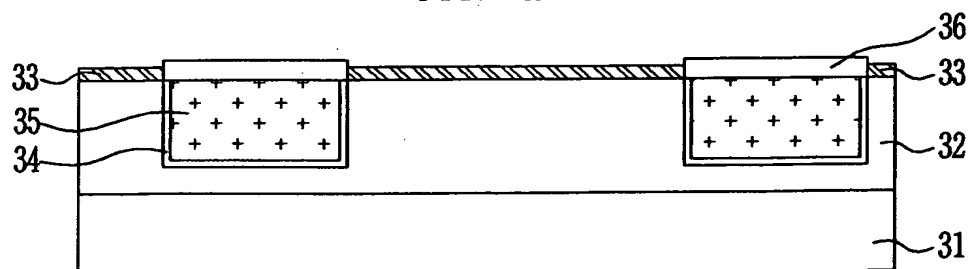


FIG. 3A



A cross-sectional view of a semiconductor device 20. The device consists of a substrate 301. On the substrate, there are two rectangular regions 302, each containing a grid of plus signs (+). These regions are surrounded by a layer 304. Above the regions 302, there is a layer 305. A thin layer 303 is positioned above the regions 302 and below the layer 305. Above the layer 303, there are two rectangular blocks 22, each containing a grid of plus signs (+). These blocks are surrounded by a layer 20b. Above the layer 20b, there are three rectangular blocks 21, each containing a grid of plus signs (+). These blocks are surrounded by a layer 20c. The top surface of the device is a flat layer 20a.

FIG. 3D

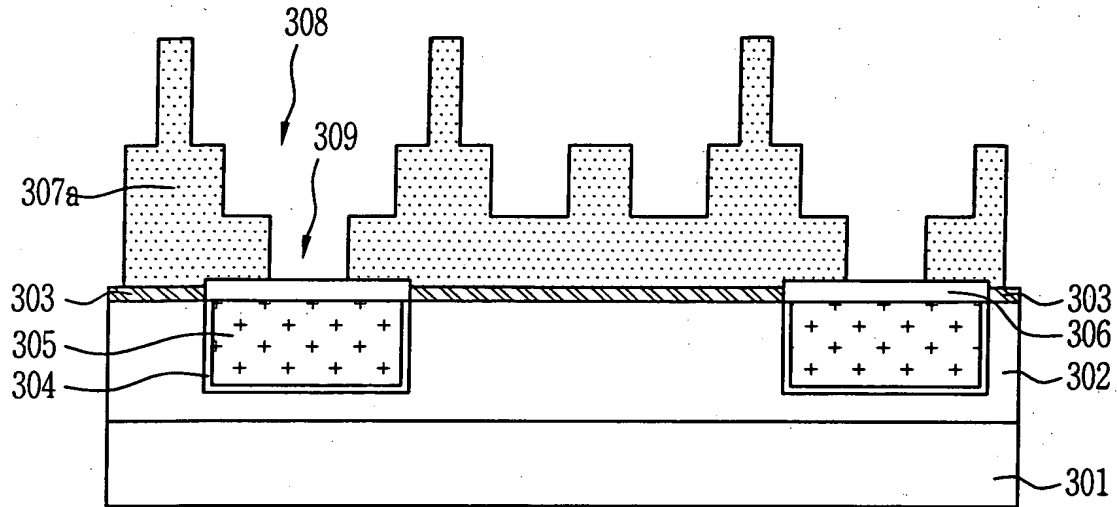


FIG. 3E

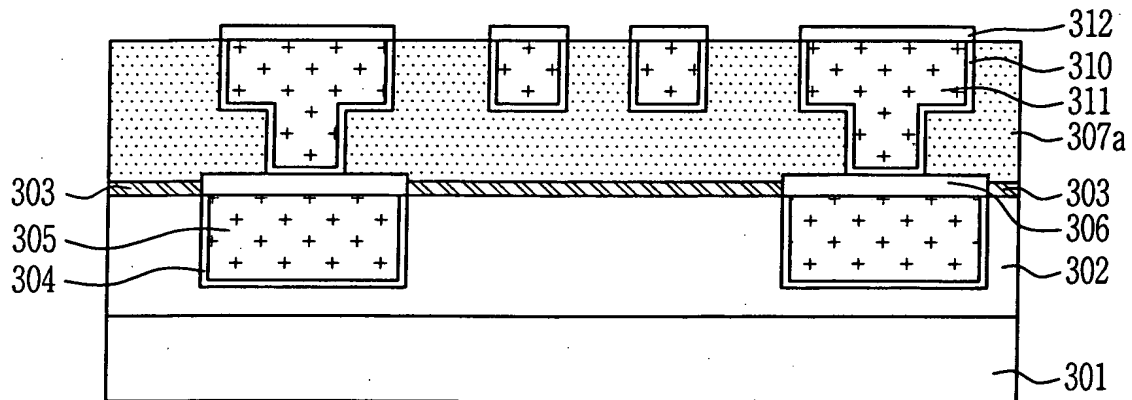


FIG. 4

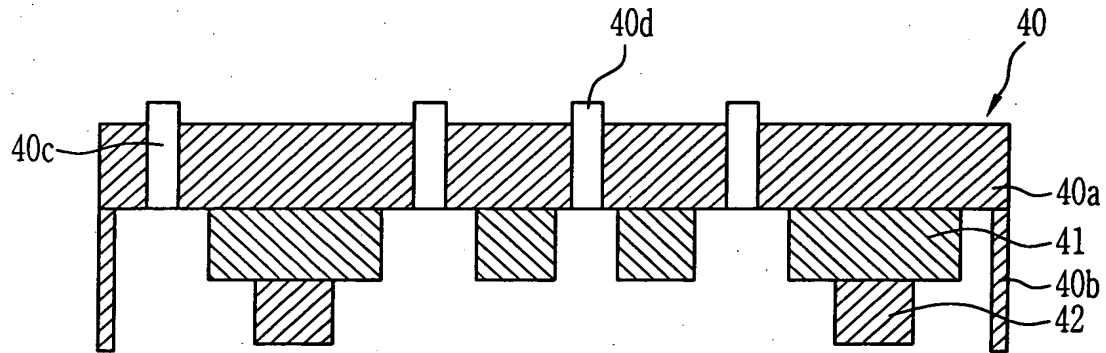


FIG. 5A

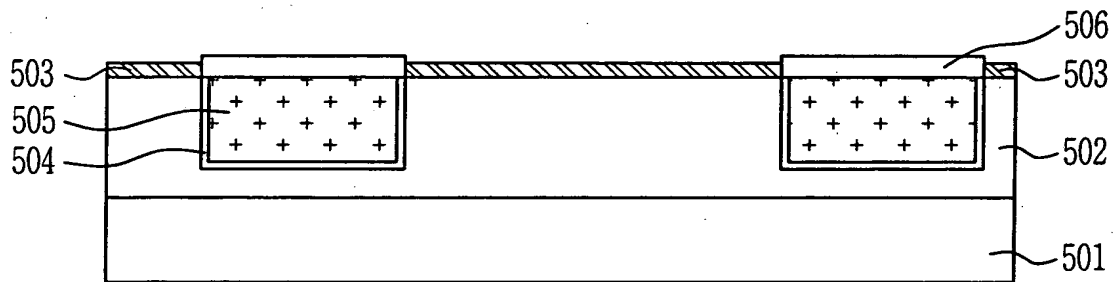


FIG. 5B

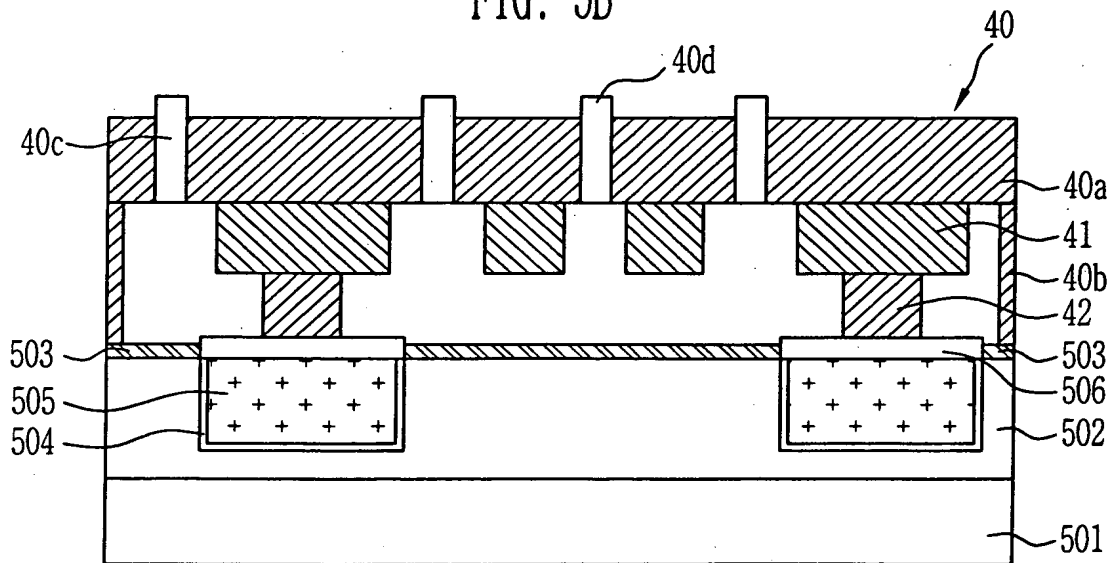


FIG. 5C

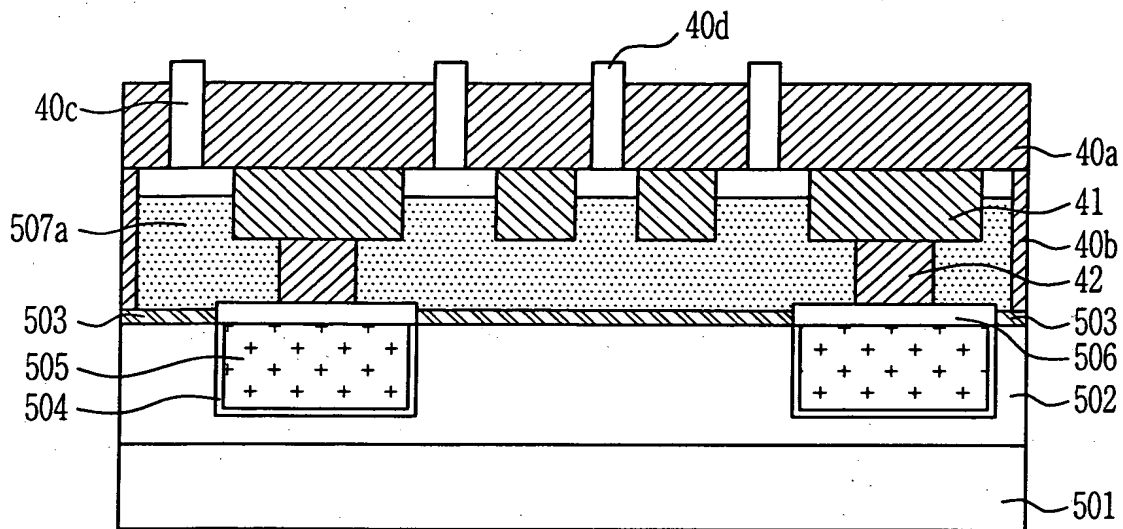


FIG. 5D

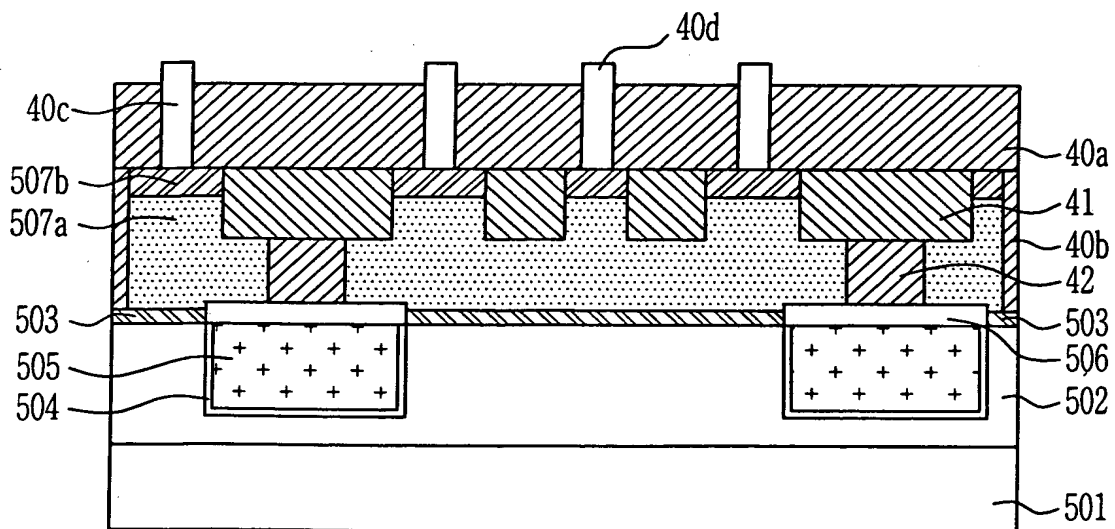


FIG. 5E

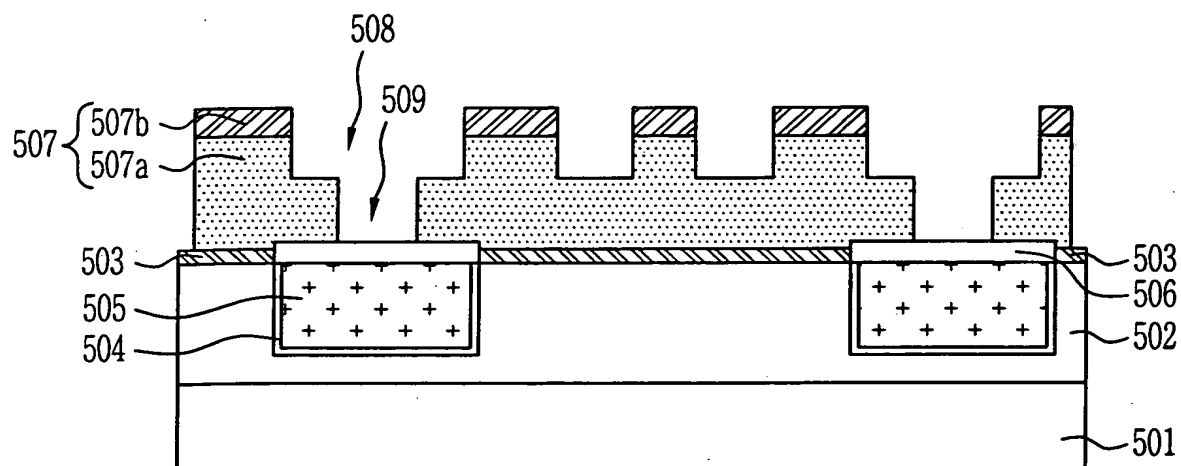


FIG. 5F

